**Lab 3: RLC Circuit Response**

**Objective:**

Introduce RLC circuits to develop a familiarity with critically damped, over-damped, under-damped situations, as well as rise time, overshoot, and settling time.

**Equipment and Components:**

* Prototyping board, Multimeter, Signal Generator, Oscilloscope.
* Resistors and/or potentiometer: value to be determined
* Inductor: 1 mH
* Capacitor: 0.01 uF

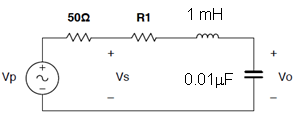
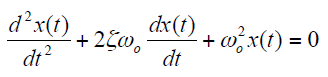


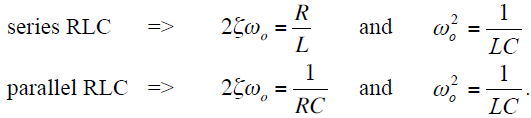
Figure 3.1: Series RLC circuit

**Background:**

All RLC circuits can be described using a general 2nd order equation that results from NODE or MESH analysis. This 2nd order equation can be rewritten in a “standard form”:



where the damping ratio (***ζ***) and the un-damped natural/resonance frequency (***ωo***) are equal to



where:

* ***α*** is the Neper frequency that measures the decay of a signal,
* ***ωo*** is the resonance frequency that the circuit would oscillate at if there were no damping, and ***ωd*** is the damped oscillation frequency.
* All of these depend upon the relationship of the resistor, inductor, and capacitor values.

***Damping Ratio*** *ζ*

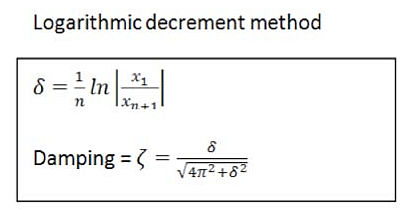
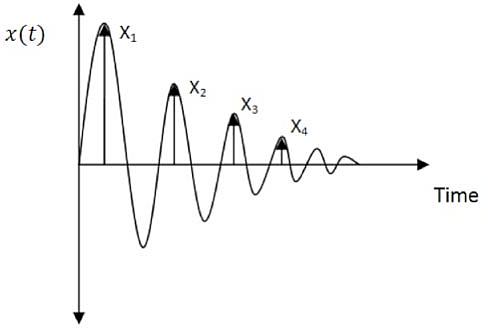
For ***ζ* > 1,** there are two distinct real roots, and the circuit is **over-damped**.

For ***ζ* = 1,** there are two real equal roots, and the circuit is **critically-damped**.

For **0 < *ζ* < 1,** there are two complex conjugate roots, and the circuit is **under-damped**.

For ***ζ* = 0,** there are two purely imaginary conjugate roots, and the circuit is **undamped (unbounded growth).**

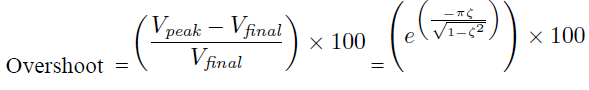
**For under-damped case:**



**Calculation of *ζ* from the under-damped response**

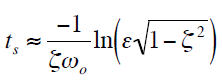
***Overshoot***

Overshoot occurs when the resistor is unable to control the flow of energy between the inductor and capacitor. The result is that the voltage and/or current can exceed the final expected value. To quantify this, we equate the percent overshoot to be



***Settling time***

When a circuit is under-damped, the damped oscillations make it difficult to identify a “final” steady state value. Instead, we define the settling time (ts) to be the amount of time it takes the voltage/current to settle to within a defined error (ε) of the final value. It is approximately the time taken by Vo to reach 10% of its final value.

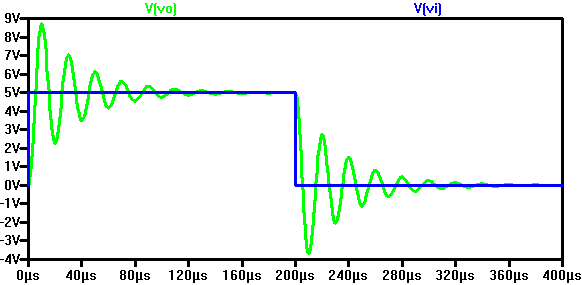
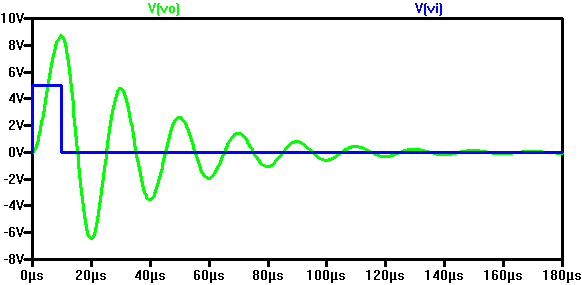


**Preliminary:**

1. For the series circuit of Figure 3.1, find the resonant frequency ωo and calculate the size of the resistance R1 that will make the circuit critically damped.

*Note: Do not forget to account for the 50 Ω source resistance (internal to the function generator that will be used to test the circuit in the lab).*

1. Approximate the value of R1 for a critically damped, under-damped and over-damped circuit.
2. Find the approximate damping ratio ζ for each R1.
3. For the underdamped case, compute the percent overshoot for Vo for the underdamped case. Also, compute the settling time for Vo to reach 10% of its final value.
4. Use Multisim or LTSpice to simulate and verify your calculation. *Hint: You can use a single pulse or step function as your input. Apply a square-wave signal as the input (for best results, use 0 to 5V square wave at 2.5 kHz; you may need to adjust the frequency to obtain a clear response). Please see Figure 3.2 below for characterizing an under-damped response.*



**(a) (b)**

**Figure 3.2: (a) Impulse and (b) step responses of an under-damped series RLC circuit**

**Procedure:**

1. Build a circuit according to Figure 3.1 with R1 being a fixed resistor plus a potentiometer. Apply a square-wave signal as the input. Monitor both input and output with the scope.
2. By adjusting the value of potentiometer, obtain and record 3 responses: critically-damped, over-damped, and under-damped, respectively. Measure and record R1 in each case.
3. For the under-damped case, measure the rise time, overshoot, and settling time.

**Conclusion:**

Use Multisim to simulate and verify your experimental results. Include a table to compare your calculated and simulated values to the measured values. Write a conclusion to discuss your observations.

**Lab 4: RLC Impedance (Matlab)**

**Objective:**

Use Matlab to plot the “impedance vs. frequency” curves for the parallel and series RLC circuits.

**Procedure:**

Write a Matlab script with the following features:

1. Let the user input the R, L, and C values.
2. Calculate the resonant frequency,.
3. Calculate the impedance for the series RLC circuit  for 
4. Calculate the impedance for the parallel RLC circuit  for 
5. Plot the curves of |ZS| vs. ω and |ZP| vs. ω (see the appendix for an example code).

**Conclusion:**

Write a report to include your code, plots, and observations (What is the minimum impedance for the series circuit? What is the maximum impedance for the parallel circuit? Do you know why?).

**Appendix**

Suggested Matlab Script (enter “help linspace” in the workspace if you don’t understand what linspace is, similarly type “help plot” and “help subplot” if you want to learn more about plotting options).

Create Lab2.m file and paste the following code.

clc %clear the workspace

clear all; %clear all previous variables in the workspace

close all; %close all the previous figures

R = input('Enter Resitance (Ohm) = ');

L = input('Enter Inductance (H) = ');

C = input('Enter Capcitance (F) = ');

w0 = 1/sqrt(L\*C)

w = linspace(0.5\*w0, 1.5\*w0);

Zs = R + j\*w\*L + 1./(j\*w\*C);

Zp = 1./(1/R + 1./(j\*w\*L) + j\*w\*C);

figure

subplot(1,2,1)

plot(w/(2\*pi),abs(Zs)),title('Series RLC Impedance'),xlabel('Frequency [Hz]'),ylabel('Magnitude [\Omega]')

subplot(1,2,2)

plot(w/(2\*pi),abs(Zp)),title('Parallel RLC Impedance'),xlabel('Frequency Hz]'),ylabel('Magnitude [\Omega]')